Claims

What is claimed is:

1. A method of providing error detection and correction in an interface between two portions of a data processing system, the method comprising:

generating, in a first portion of the data processing system, parity bits corresponding to substantially the entirety of bits contained in the interface;

transmitting across the interface the parity bits together with the entirety of bits contained in the interface;

testing, in a second portion of the data processing system, that the parity bits correspond to the bits for which parity was encoded; and

detecting and correcting, in a second portion of the data processing system, errors in the bits for which parity was encoded.

2. The method according to claim 1 wherein the interface is a connector.

3. The method according to claim 1 wherein the interface includes data, address and control signals.

4. The method according to claim 1 wherein an indication is provided to the data processing system of corrected errors.

5. The method according to claim 1 wherein an indication is provided to the data processing system of uncorrected errors.

6. The method according to claim 1 wherein single bit errors are detected and corrected.

7. A system for error detection and correction in an interface between two portions of a data processing system, the system comprising:

a parity generator, in a first portion of the data processing system, for generating parity bits corresponding to substantially the entirety of bits contained in the interface;

an interface for transmitting the data bits and the parity bits;

a parity checker, in a second portion of the data processing system, for checking that the parity bits correspond to the bits for which parity was encoded; and

an error correction circuit, in a second portion of the data processing system, for correcting errors in the bits for which parity was encoded.

8. The system according to claim 7 wherein the interface is a connector.

9. The system according to claim 7 wherein the interface includes data, address and control signals.

10. The system according to claim 7 wherein an indication is provided to the data processing system of corrected errors.

11. The system according to claim 7 wherein an indication is provided to the data processing system of uncorrected errors.

12. The method according to claim 7 wherein single bit errors are detected and corrected.

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